

SEMICONDUCTOR ARRANGEMENT WITH COVERED ISLAND AND CONTACT REGIONS

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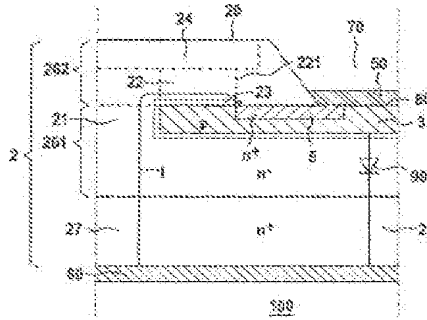
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JP4210110 (B2)
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Abstract not available for JP 2004505453 (T)

Abstract of corresponding document: **WO 0209195 (A1)**

The invention relates to a semiconductor arrangement for current control, comprising an n-type first semiconductor region (2) with a first surface (20), a p-type covered island region (3), within the first semiconductor region (2), with a second surface (80), an n-type contact region (5) arranged on the second surface (80) within the island region (3) and a lateral channel region (22), formed between the first and second surface (20 and 80) as part of the first semiconductor region (2). Said channel region is part of a current path from or to the contact region (5). The current (I) within the lateral channel region (22) may be influenced by at least one depleted zone (23, 24). A lateral edge (221) of the lateral channel region (22) extends as far as the contact region (5).



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